WHAT IS CLAIMED IS:

1. A microprocessor comprising:

a CPU which performs certain arithmetic operations;

an address bus connected to the CPU;

a circuit unit which utilizes an address on the address bus; and

a test circuit which generates a test address for testing the circuit unit.

2. The microprocessor as claimed in claim 1, further comprising a brake mechanism which comprises:

a plurality of comparators which compare addresses supplied;

a control register which receives the outputs of the plurality of comparators; and

a brake request generator which outputs a brake request to the CPU in accordance with a control signal supplied from the control register.

3. The microprocessor as claimed in claim 1, wherein the test circuit comprises:

a control circuit which contains a register storing control values;

an address decoder which receives the control values from the control circuit;

a bit pattern register which generates a bit pattern to produce a test address;

a rotator which makes a change to the bit pattern; and

a bus driver which receives the test address and drives the address bus.

4. The microprocessor as claimed in claim 1, further comprising a test result holding register which holds test results and comprises:

a comparison result determination circuit which compares actual test results with expected values;

a flag register which receives and stores the output of the comparison result determination circuit; and

a control circuit which controls the comparison result determination circuit and the flag register.

5. A microprocessor comprising:

a CPU which performs certain arithmetic operations;

an instruction bus which is connected to the CPU and includes an instruction address bus and an instruction data bus;

a circuit unit which can be tested with the use of an address on the instruction address bus; and

a test circuit which inputs a return instruction into the CPU via the instruction data

bus when receiving a branch instruction from the CPU in an initial state immediately after actuation.

6. A microprocessor comprising:

a program for fetching an instruction at a predetermined address, and executing an instruction to carry out an unconditional return without using a code at a branch destination as an instruction after a branch occurs to a designated address.

7. A microprocessor comprising:

a CPU having an instruction bus and a data bus which are independent of each other,

wherein

an instruction to make data read access to the instruction bus is issued.